CLAIMS

1. A method for semiconductor process chamber operation, comprising:

depositing a silicon containing layer over an inner surface of an empty semiconductor process chamber;

introducing a wafer into the semiconductor process chamber after depositing the silicon containing layer;

performing a process operation on the wafer, the process operation depositing a residue on the silicon containing layer covering the inner surface of the semiconductor process chamber;

removing the wafer from the semiconductor process chamber; and

initiating an in-situ cleaning process upon completion of the processing operation and removal of the wafer, the initiating including:

flowing a fluorine containing gas into the semiconductor process chamber; and

establishing a pressure within the semiconductor process chamber capable of allowing a plasma created from the fluorine containing gas to clear the silicon containing layer covering the inner surface of the processing chamber.

2. The method of claim 1, wherein the method operation of initiating an in-situ cleaning process upon completion of the processing operation and removal of the wafer further includes;

flowing an oxygen containing gas into the semiconductor process chamber while maintaining the pressure; and

creating a plasma from the oxygen containing gas to remove carbon based byproducts deposited on the silicon containing layer.

3. The method of claim 1, wherein the process operation is selected from the group consisting of an silicon etch operation, polysilicon etch operation, mask open operation, via etch, contact etch, aluminum metal etch, tungsten etch back, and metal gate etch.

4. The method of claim 1, wherein the pressure is about 250 milliTorr (mT)

5. The method of claim 1, wherein the fluorine containing gas includes oxygen for removal of carbon based byproducts.

6. The method of claim 1 further including:

defining process parameters including a temperature of the processing chamber, a power applied to a transformer coupled plasma (TCP) coil, and a flow rate of the fluorine containing gaseous mixture.

7. The method of claim 6, wherein the temperature is about 60°C, the power is about 800 watts, and the flow rate is between about 100 and about 500 standard cubic centimeters per minute (sccm).

8. The method of claim 1, wherein the method operation of depositing a silicon containing layer over an inner surface of a semiconductor process chamber includes,

creating a plasma while flowing a silicon containing gas into the semiconductor process chamber.

9. The method of claim 8, wherein the silicon containing gas is selected from the group consisting of SiH_4, Si_2H_6, SiH_3CH_3, $Si(CH_3)_3$, SiF_4, $SiCl_4$, $SiHCl_3$, SiH_2Cl_2, $SiBr_4$ and TEOS.

10. A method for cleaning and pre-coating a process chamber to provide substantially similar starting conditions for each process operation, comprising:

depositing a silicon containing pre-coat over the inner surfaces of a process chamber;

introducing a wafer into the process chamber;

performing a process operation on the wafer,

depositing CF_x residues on the silicon containing pre-coat over the inner surfaces of the process chamber as part of the process operation;

removing the wafer from the process chamber; and

performing an oxygen plasma cleaning operation to remove the CF_x residues deposited from the process operation.

11. The method of claim 10, wherein the method operation of performing an oxygen plasma cleaning operation includes,

creating an oxygen plasma while flowing oxygen into the process chamber; and

releasing fluorine from the CF_x residues by reacting oxygen of the oxygen plasma with carbon of the CF_x residues, wherein the releasing fluorine aids in clearing the silicon coated inner surfaces.

12. The method of claim 10 wherein the process operation is selected from the group consisting of an silicon etch operation, polysilicon etch operation, mask open operation, via etch, contact etch, aluminum metal etch, tungsten etch back, and metal gate etch.

13. The method of claim 10, further comprising:

introducing $SiCl_4$ into the process chamber;

striking a plasma while introducing the $SiCl_4$ into the process chamber; and

forming the silicon containing pre-coat having about a 50 Å to about a 4000 Å thickness.

14. The method of claim 10, further comprising:

performing a fluorine plasma cleaning operation prior to the oxygen plasma cleaning operation.

15. A semiconductor processing chamber, comprising:

a top electrode in communication with a power supply; and

a processing chamber defined within a base, a sidewall extending from the base, and a top disposed on the sidewall, the processing chamber having an outlet enabling removal of fluids within the processing chamber, the processing chamber including,

a substrate support; and

an inner surface of the processing chamber defined by the base, the sidewall and the top, the inner surface being coated with a removable silicon

containing coating, the silicon containing coating configured to seal particles between the inner surface and the silicon containing coating.

16. The semiconductor processing chamber of claim 15, wherein the silicon coating prevents transfer of metal contaminants from the inner surface of the chamber to a wafer during a processing operation.

17. The semiconductor processing chamber of claim 15, wherein the silicon coating has a thickness of between about 50 angstroms (Å) and about 4000Å.

18. The semiconductor processing chamber of claim 15, wherein the silicon containing coating is distributed over the inner surface by creating a silicon containing plasma within the semiconductor processing chamber.

19. The semiconductor processing chamber of claim 15, wherein the silicon containing coating is removed and reapplied after completion of each process operation within the semiconductor processing chamber.